

The Linnet logo features the word "Linnet" in a bold, black, sans-serif font. Above the letters "i" and "n" are four small blue squares arranged in a horizontal row. A blue horizontal bar is positioned below the text, with a curved cutout on the right side.

**Data Sheet of
Linnet Controller Device
LN2007**

*Rev. 0.1
Date: 16.09.2003*

1 Overview

Device's pin names are referred with **BOLDFACE** symbols in this document. Register names are referred using *THIS* or *THIS*.

2 Pin description

LN2007 is assembled to 100 pin TQFP package. Following table describes the pin characteristics.

PIN NBR.	PIN NAME	PIN TYPE ⁽¹⁾	PULL UP/ DOWN ⁽²⁾	PIN description
1	DAC7	O		LINET output voltage drive value, bit 7 = MSB.
2	DAC6	O		LINET output voltage drive value, bit 6.
3	DAC5	O		LINET output voltage drive value, bit 5.
4	DAC4	O		LINET output voltage drive value, bit 4.
5	GND	P		0 V.
6	GND	P		0 V.
7	DAC3	O		LINET output voltage drive value, bit 3.
8	DAC2	O		LINET output voltage drive value, bit 2.
9	DAC1	O		LINET output voltage drive value, bit 1.
10	DAC0	O		LINET output voltage drive value, bit 0 = LSB.
11	PWR	O		LINET driver supply control, 1 = supply enabled.
12	PWM	O		Pulse width modulated bit stream. Stream length 256 cycles of CLK .
13	VCC	P		3.3 V Supply voltage.
14	VCC	P		3.3 V Supply voltage.
15	TEMP	O		Measurement switch control selecting temperature (<i>MSRT</i>). ⁽³⁾
16	VOLT	O		Measurement switch control selecting voltage (<i>MSRS</i> , <i>MSRP</i>). ⁽³⁾
17	CURR	O		Measurement switch control selecting current (<i>IDLE0</i> , <i>IDLE1</i> , <i>FIDVAL</i>). ⁽³⁾
18	INTEGR	O		Current measurement integration switch control (<i>IDLE0</i> , <i>IDLE1</i> , <i>FIDVAL</i>). ⁽³⁾
19	CLKAD	O		Analog to digital converter clock. Frequency 5 MHz when parallel converter mode selected with <i>MODEREG/CIM</i> , else 2.5 MHz.
20	ADCMSB	BID		Bit 11 (MSB) of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> . CONV bit source in LTC1401 mode.
21	ADC0	I		Bit 0 (LSB) of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> . Conversion data in LTC1401 mode.
22	ADC1	I	U	Bit 1 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> .
23	ADC2	I	U	Bit 2 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> .
24	GND	P		0 V.
25	GND	P		0 V.
26	ADC3	I	U	Bit 3 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> .
27	ADC4	I	U	Bit 4 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> .
28	ADC5	I	U	Bit 5 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> .
29	ADC6	I	U	Bit 6 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> .
30	VCC	P		3.3 V Supply voltage.
31	VCC	P		3.3 V Supply voltage.
32	ADC7	I	U	Bit 7 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> .
33	ADC8	I	U	Bit 8 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM</i> .
34	ADC9	I	U	Bit 9 of analog to digital converter when parallel converter mode selected with

⁽¹⁾Pin types: **BID** = BI-Directional
 I = Input
 O = Output
 P = Power/Ground

⁽²⁾Pull symbols: **U** = Up
 D = Down

⁽³⁾Active polarity defined with *MODEREG/SWOFF*

PIN NBR.	PIN NAME	PIN TYPE ⁽¹⁾	PULL UP/ DOWN ⁽²⁾	PIN description
				<i>MODEREG/CIM.</i>
35	ADC10	I	U	Bit 10 of analog to digital converter when parallel converter mode selected with <i>MODEREG/CIM.</i>
36	INA	I	U	Inverter in.
37	nA	O		Inverter out (not INA).
38	GND	P		0 V.
39	GND	P		0 V.
40	LED1	O		LED driver (<i>LED</i>).
41	LED2	O		LED driver (<i>LED</i>).
42	RES_OUT	O		Inverted nRESET.
43	GPIO3	BID	D	General purpose Input/Output, see <i>GPE, GPO, GPI.</i>
44	GPIO2	BID	D	General purpose Input/Output, see <i>GPE, GPO, GPI.</i>
45	VCC	P		3.3 V Supply voltage.
46	VCC	P		3.3 V Supply voltage.
47	GPIO1	BID	D	General purpose Input/Output, see <i>GPE, GPO, GPI.</i>
48	GPIO0	BID	D	General purpose Input/Output, see <i>GPE, GPO, GPI.</i>
49	nRESET	I		Reset, low active.
50	DI_ALL	O		Detected LINET data in.
51	GND	P		0 V.
52	GND	P		0 V.
53	AD_STR	O		Analog to digital conversion integration active when high. ⁽⁴⁾
54	FID0STR	O		Frame ID #0 position when high. ⁽⁴⁾
55	FIDSTR	O		Selected (<i>FID</i>) Frame ID position when high. ⁽⁴⁾
56	DO	BID	D	Bit 7 of <i>HWID</i> / Data out for selected (<i>FID</i>) Frame ID. ⁽⁴⁾
57	DI	BID	D	Bit 6 of <i>HWID</i> / Data in from selected (<i>FID</i>) Frame ID. See also <i>FIDVAL</i> . ⁽⁴⁾
58	FID0I	BID	D	Bit 5 of <i>HWID</i> / Data in from at Frame ID=0. ⁽⁴⁾
59	S5	BID	D	Bit 4 of <i>HWID</i> / Service command bit 5. ⁽⁴⁾
60	VCC	P		3.3 V Supply voltage.
61	VCC	P		3.3 V Supply voltage.
62	S4	BID	D	Bit 3 of <i>HWID</i> / Service command bit 4. ⁽⁴⁾
63	S3	BID	D	Bit 2 of <i>HWID</i> / Service command bit 3. ⁽⁴⁾
64	S2	BID	D	Bit 1 of <i>HWID</i> / Service command bit 2. ⁽⁴⁾
65	S1	BID	D	Bit 0 of <i>HWID</i> / Service command bit 1. ⁽⁴⁾
66	INT	O		Frame interrupt (<i>FrameINT</i>), high active, generated just before Frame ID=0.
67	nWR	I		uP write strobe, low active.
68	nRD	I		uP read strobe, low active.
69	nCSM	I		Buffer memory select by uP, low active.
70	GND	P		0 V.
71	GND	P		0 V.
72	NC ⁽⁵⁾			
73	GND	P		0 V.
74	NC ⁽⁵⁾			
75	NC ⁽⁵⁾			
76	nCS	I		Register space select by uP, low active.
77	D7	BID		uP data bit 7 (MSB).
78	D6	BID		uP data bit 6.
79	D5	BID		uP data bit 5.
80	D4	BID		uP data bit 4.
81	D3	BID		uP data bit 3.
82	VCC	P		3.3 V Supply voltage.
83	D2	BID		uP data bit 2.
84	D1	BID		uP data bit 1.
85	D0	BID		uP data bit 0 (LSB).
86	A0	I		uP address bit 0 (LSB).
87	A1	I		uP address bit 1.
88	A2	I		uP address bit 2.
89	A3	I		uP address bit 3.
90	VCC	P		3.3 V Supply voltage.
91	A4	I		uP address bit 4.
92	A5	I		uP address bit 5.
93	A6	I		uP address bit 6.
94	GND	P		0 V.
95	A7	I		uP address bit 7 (MSB).
96	GND	P		0 V.
97	CLK	I		10 MHz system clock.
98	CKI	I	D	General purpose clock in.
99	CK/2	O		CKI/2.
100	CK/4	O		CKI/4.

Table 1 LN2007 pin description list.

⁽⁴⁾Debug information from LINET traffic

⁽⁵⁾Pins named with NC symbol should be left open

3 Microprocessor interface

Microprocessor sees LN2007 as two separate address spaces:

- buffer memory space (section 3.2) pointed by **nCSM** terminal and
- register space (section 3.3) pointed by **nCS**

Detailed timing for microprocessor transactions is presented in section 3.1.

3.1 Microprocessor interface timing

Microprocessor interface timing parameters are introduced in the figures Figure 1 and Figure 2.

Note that only one of chip selects **nCS** and **nCSM** is allowed to be active (low) in time. Note also that **nRD** is high (passive) for whole write cycle and **nWR** for whole read cycle.

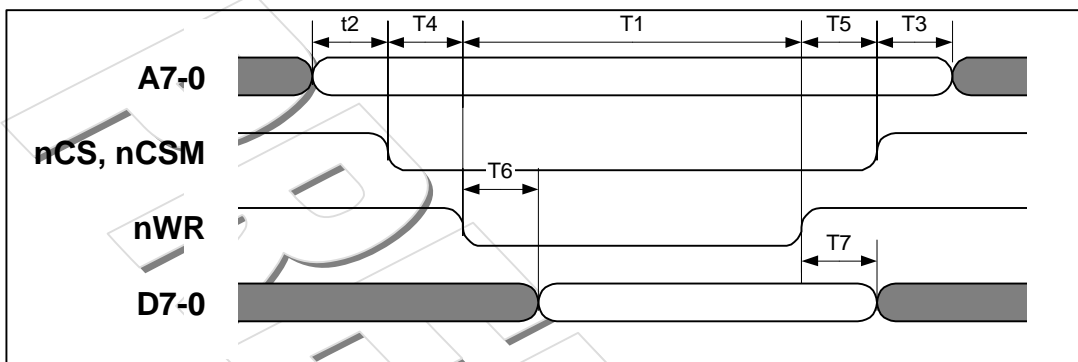


Figure 1 Write timing

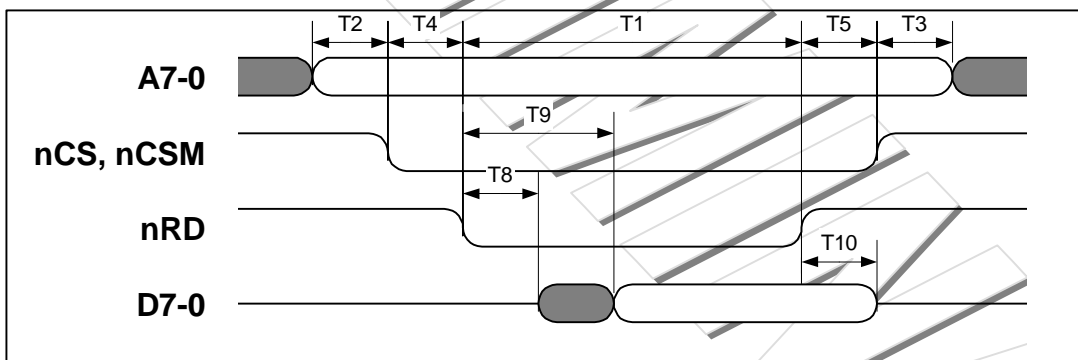


Figure 2 Read timing

Symbol	Parameter	Min	Typ	Max
T1	nWR, nRD width	250		
T2	Address setup to nCS, nCSM active	0		
T3	Address hold time from nCS, nCSM	0		
T4+T5	Transaction passive time	25		
T6	Data valid after nWR active edge			10
T7	Data hold from nWR passive edge	0		

T8	Data turned driving from nRD active edge			10
T9	Data valid from nRD active edge			150
T10	Data turned high impedance from nRD passive edge			10

Table 2 Microprocessor interface timing parameters

3.2 Buffer memory space

Microprocessor uses buffer memory space for exchanging data between Linet network units. This space consists of a space from 0x00 to 0xFF selected by **nCSM**. It is divided into four pages both for input (receiving from network) and output (sending to network). Each page consists of 32 bytes Frame ID 0 aligned to bit 0 of first byte, Frame ID 8 to bit 0 of second byte etc. First four frames are allocated for input buffers and rest for output buffers. Each buffer carries valid data up to the frame alignment word consisting of a bit stream of zero followed by six ones ("0111111") at the end of frame. In addition, Frame ID 0 positions in output buffers are discarded.

Microprocessor provides the page numbers for LN2007 internal logic in the *IPAGE* and *OPAGE* fields of *BUFPAGE* register. Internal logic samples these fields at the beginning of the frame alignment word that takes place prior to *FrameINT* interrupt. At this point previous input frame has been stored to buffer sampled last time from *IPAGE* and output frame pointed by last sample of *OPAGE* has already used.

3.3 Register space

LN2007 registers are listed in the following lines divided to chapters by their widths and modes. Each register is described in it's own structure table consisting of one header box and one or more description boxes as follows:

Address	Register name	Register title	
Bit range	Field name ⁽⁶⁾	Field mode ⁽⁷⁾ Reset value ⁽⁸⁾	Register/field description.
0 or more additional field description boxes			

Table 3 Example of register structure.

uP activates operations to these registers with low polarity in **nCS**.

3.3.1 Read/write registers, byte wide

0x00	<i>ASICID</i>	ASIC Identification register	
7-0		R/W	0x07 Returns the value written here XOR'ed with 0x7. For example: written 0xFF => returned 0xF1.
0x01	<i>FID</i>	Frame ID selected for motoring	
7-0		R/W	0x00 Debug source for DI , DO and FIDSTR is selected using this register. See also: <i>FIDVAL</i> .
0x02	<i>FrameINT</i>	Frame Interrupt Status/ack	

⁽⁶⁾Field name is left blank with register structures having only one description box.

⁽⁷⁾Field modes: R = Read
W = Write

R/W = Read and Write

⁽⁸⁾Undeclared register bits and fields with 'W' mode return 0.

0	R/W	'0'	Read: '1' = Frame interrupt pending. Write: '1' => '1' returned unconditionally. Write: '0' => '0' returned provided that FrameInt is not getting active in the same time. Note that FrameINT returns INT0 pin value.
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0x03	MODEREG	Main mode control register		
0	INIT	R/W	'1'	Initialization mode: UP has access to wave ram. Power down state driven unconditionally. See also <i>ORMAN/PD</i> .
1	DCMODE	R/W	'0'	DC mode: DAC7-0 driven with value of <i>DCVAL</i> .
2	CIM	R/W	'0'	Current integration mode: 0' = internal mode using parallel ADC. 1' = external mode using LTC1401 serial ADC.
	3SWOFF	R/W	'0'	Analog switch off polarity: 0' = off with low control voltage.

0x04	WAVED	Wave data		
7-0		R/W	0x00	uP accesses data to/from wave memory through this register. See also <i>WAVEA</i> .

0x05	DCVAL	DC value source		
7-0		R/W	0x80	Value driven to DAC7-0 when <i>MODEREG/DCMODE</i> active.

0x06	BUFPAGE	Buffer page selection		
1-0	OPAGE	R/W	1	Output page.
3-2	IPAGE	R/W	0	Input page.

0x07	LED	LED Control		
0	LED1	R/W	'0'	Inversion of this bit fed to LED1 pin.
1	LED2	R/W	'0'	Inversion of this bit fed to LED2 pin.

0x08	LSTFID	Last Frame ID		
7-0		R/W	252	Frame length selection: Frame length = <i>LSTFID</i> +1.

0x09	PWM	PWM output control		
7-0		R/W	0x00	Pulse width modulated output control. 0x00 = all zero fed out from PWM pin.

0x0A	CSUMDLY	Current integration delay		
7-0		R/W	12	Current integration delay from theoretical center when <i>MODEREG/CIM</i> bit set active.

0x0B	CSUMDEV	Current integration deviation		
7-0		R/W	32	Current integration deviation when <i>MODEREG/CIM</i> bit set active.

0x0C	ORMAN	Over Range Management		
0	ORP_K	R/W	'1'	'1' = Keep '1' in <i>ORP_PS</i> . '0' = Force <i>ORP_PS</i> to '0' unconditionally.
1	ORS_K	R/W	'1'	'1' = Keep '1' in <i>ORS_PS</i> . '0' = Force <i>ORS_PS</i> to '0' unconditionally.
2	ORT_K	R/W	'1'	'1' = Keep '1' in <i>ORT_PS</i> . '0' = Force <i>ORT_PS</i> to '0' unconditionally.
3	PD	R/W	'1'	'1' = SW Power Down unconditionally. See also <i>MODEREG/INIT</i> . Note that Power Down state means that PWR_ON output is forced to '0' and all '0's fed to DAC7-0 pins.
4	ORP_E	R/W	'1'	'1' = Enable HW Power Down by '1' in <i>ORP_PS</i> . See also <i>PD</i> bit.
5	ORS_E	R/W	'1'	'1' = Enable HW Power Down by '1' in <i>ORS_PS</i> . See also <i>PD</i> bit.
6	ORT_E	R/W	'1'	'1' = Enable HW Power Down by '1' in <i>ORT_PS</i> . See also <i>PD</i> bit.

0x0D	GPO	General purpose output Data		
0	GPO0	R/W	'0'	GPIO0 pin output data. See also <i>GPE/GPE0</i>
1	GPO1	R/W	'0'	GPIO1 pin output data. See also <i>GPE/GPE1</i>
2	GPO2	R/W	'0'	GPIO2 pin output data. See also <i>GPE/GPE2</i>
3	GPO3	R/W	'0'	GPIO3 pin output data. See also <i>GPE/GPE3</i>
4	GPO0M	W ⁽⁵⁾	'0'	<i>GPO0</i> write mask: '1' = write enabled
5	GPO1M	W ⁽⁵⁾	'0'	<i>GPO1</i> write mask: '1' = write enabled
6	GPO2M	W ⁽⁵⁾	'0'	<i>GPO2</i> write mask: '1' = write enabled
7	GPO3M	W ⁽⁵⁾	'0'	<i>GPO3</i> write mask: '1' = write enabled

0x0E	GPE	General purpose output Enable		
0	GPE0	R/W	'0'	GPIO0 pin output enable. '1' = enabled
1	GPE1	R/W	'0'	GPIO1 pin output enable. '1' = enabled
2	GPE2	R/W	'0'	GPIO2 pin output enable. '1' = enabled
3	GPE3	R/W	'0'	GPIO3 pin output enable. '1' = enabled
4	GPE0M	W ⁽⁵⁾	'0'	<i>GPE0</i> write mask: '1' = write enabled
5	GPE1M	W ⁽⁵⁾	'0'	<i>GPE1</i> write mask: '1' = write enabled
6	GPE2M	W ⁽⁵⁾	'0'	<i>GPE2</i> write mask: '1' = write enabled
7	GPE3M	W ⁽⁵⁾	'0'	<i>GPE3</i> write mask: '1' = write enabled

3.3.2 Read registers, byte wide

0x10	REJECT	Frame Reject status		
0		R	X	Returns '1' if any of mandatory '0' positions is found with '1' input data during one frame. State is updated immediately before FrameINT activation moment.

0x11	ORSTAT	Over Range Status		
0	ORP_PS	R	X	Power half out of range detection. Source for HW power down processing. It is forced to '0' as long as ORP_K carries '0', which means that over range processing is inhibited on it's behalf. See also THRP and MSRP . '1' = Power half voltage found out of limits at least in two successive frames. Note that '1' is kept as long as ORP_K carries '1'.
1	ORS_PS	R	X	Signal half out of range detection. Source for HW power down processing. It is forced to '0' as long as ORS_K carries '0', which means that over range processing is inhibited on it's behalf. See also THRS and MSRS . '1' = Signal half voltage found out of limits at least in two successive frames. Note that '1' is kept as long as ORS_K carries '1'.
2	ORT_PS	R	X	Temperature out of range detection. Source for HW power down processing. It is forced to '0' as long as ORT_K carries '0', which means that over range processing is inhibited on it's behalf. See also THRT and MSRT . '1' = Temperature found out of limits at least in two successive frames. Note that '1' is kept as long as ORT_K carries '1'.
4	ORP_S	R	X	Power half out of range status. Updated once in frame at the second frame word bit. See also THRP and MSRP . '1' = Power half voltage found out of limits.
5	ORS_S	R	X	Signal half out of range status. Updated once in frame at the second frame word bit. See also THRS and MSRS . '1' = Signal half voltage found out of limits.
6	ORT_S	R	X	Temperature out of range status. Updated once in frame at the second frame word bit. See also THRT and MSRT . '1' = Temperature found out of limits.

0x12	HWID	Hardware Identification		
7-0		R	X	Returns a vector formed by DO, DI, FID0I, S5-0 pins so that DO is the MSB and S0 is the LSB. Vector is latched when MODEREG/INIT bit is high turning pins in question as inputs.

0x13	GPI	General purpose input		
0	GPI0	R	X	GPI00 pin state.
1	GPI1	R	X	GPI01 pin state.
2	GPI2	R	X	GPI02 pin state.
3	GPI3	R	X	GPI03 pin state.

3.3.3 Read/write registers, two bytes wide

0x20	WAVEA	Wave address		
8-0		R/W	0x000	Address for uP operations to wave memory. Value is incremented after every operation to WAVED register.

0x22	THRESHOLD	Input data decision threshold		
15-0		R/W	0x032	Decision threshold for input data. Value represents the level over measured base levels IDLE0 and IDLE1 for '0' and '1' output data respectively. Input data is considered to be '1' if the measured value is bigger than IDLE?" + THRESHOLD . '?' Stands for '0' or '1' output data at the decision moment.

0x24	THRP	Power Half Threshold		
11-0		R/W	0xFFFF	Decision threshold for HW power down processing from power half detection. Levels over this threshold are considered as out of range values. See also ORSTAT and MSRP .

0x26	THRS	Signal Half Threshold		
11-0		R/W	0x000	Decision threshold for HW power down processing from signal half detection. Levels under this threshold are considered as out of range values. See also ORSTAT and MSRS .

0x28	THRT	Temperature Threshold		
11-0		R/W	0xFFFF	Decision threshold for HW power down processing from temperature detection. Levels over this threshold are considered as out of range values. See also ORSTAT and MSRT .

3.3.4 Read registers, two bytes wide

0x30	<i>FIDVAL</i>	Measured current at FID		
15-0		R	X	Measured current at <i>FID</i> .

0x32	<i>IDLE0</i>	Measured base level at '0' output data		
15-0		R	X	Measured and filtered base level current at '0' output data. Measurement is carried out at the data '0' cycle before frame word.

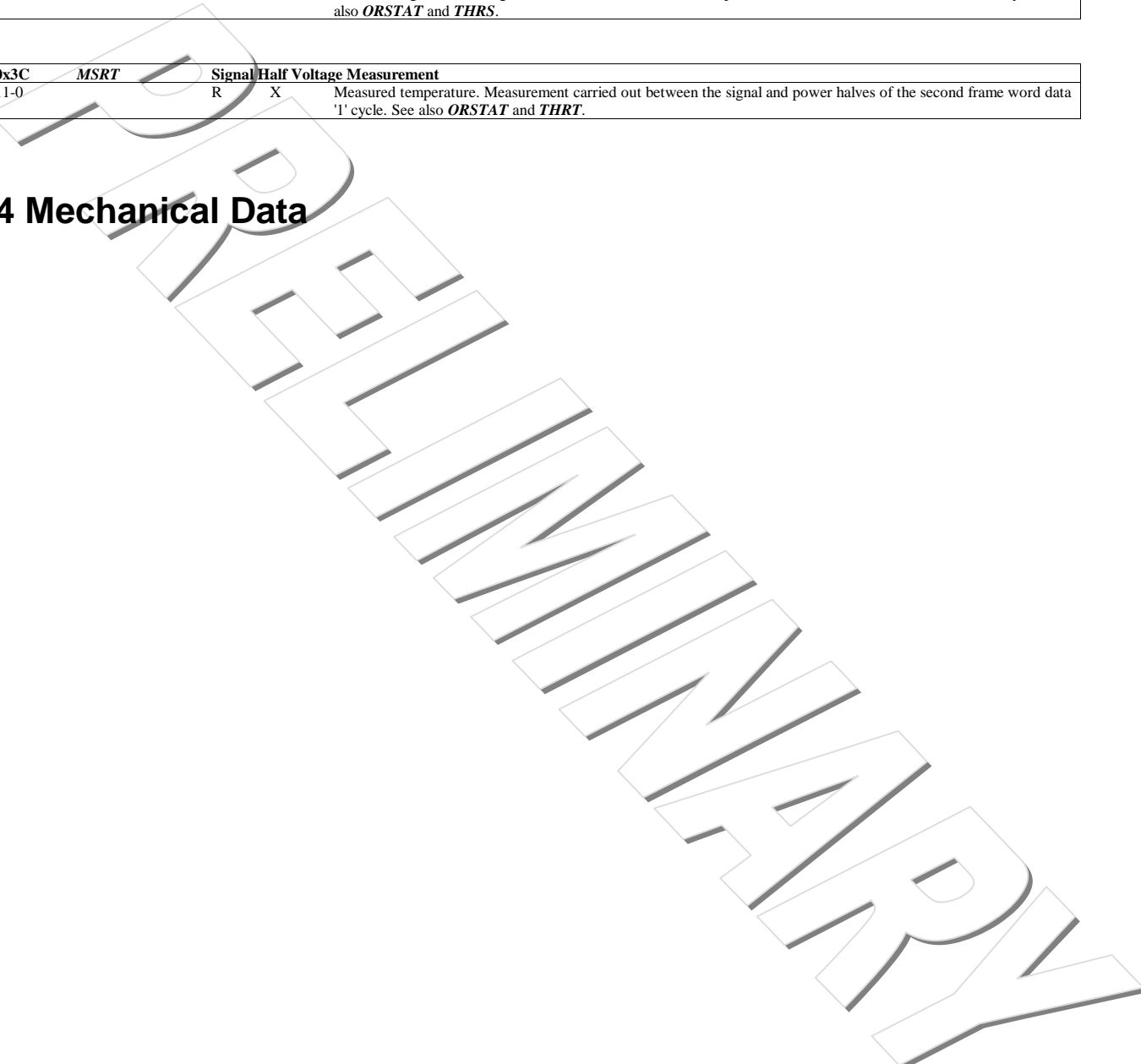
0x34	<i>IDLE1</i>	Measured base level at '1' output data		
15-0		R	X	Measured and filtered base level current at '1' output data. Measurement carried out at the first frame word data '1' cycle.

0x38	<i>MSRP</i>	Power Half Voltage Measurement		
11-0		R	X	Measured power half voltage. Measurement carried out at the power half of the second frame word '1'. See also <i>ORSTAT</i> and <i>THRP</i> .

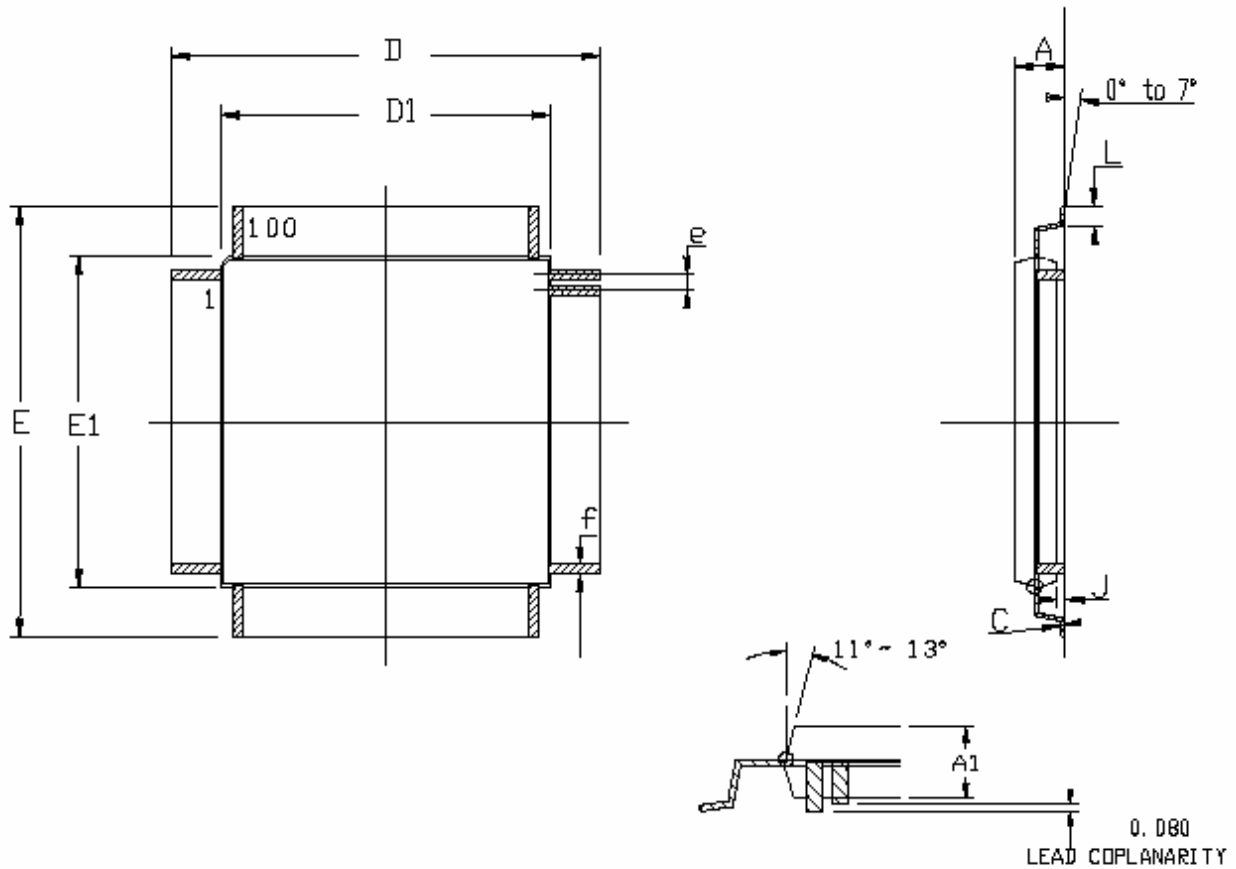
0x3A	<i>MSRS</i>	Signal Half Voltage Measurement		
11-0		R	X	Measured signal half voltage. Measurement carried out at the power half of the second frame word data '1' cycle. See also <i>ORSTAT</i> and <i>THRS</i> .

0x3C	<i>MSRT</i>	Signal Half Voltage Measurement		
11-0		R	X	Measured temperature. Measurement carried out between the signal and power halves of the second frame word data '1' cycle. See also <i>ORSTAT</i> and <i>THRT</i> .

4 Mechanical Data



100 LBS THIN QUAD FLAT PACK



	MM		INCH	
	Min	Max	Min	Max
A	----	1.20	----	.047
A1	0.95	1.05	.037	.041
C	0.09	0.20	.004	.008
D	16.00 BSC		.630 BSC	
D1	14.00 BSC		.551 BSC	
E	16.00 BSC		.630 BSC	
E1	14.00 BSC		.551 BSC	
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.50 BSC		.020 BSC	
f	0.17	0.27	.007	.011

Figure 3. Mechanical data for TQFP 100 package

